AMENDMENTS TO THE CLAIMS

Please amend the claims as set forth in the following listing. This listing of claims will replace all prior versions, and listings, of claims for the present application:

Claims 1-54 (Canceled).

55.(Amended) A process for using a photo-definable layer in a ~~positive~~ negative mask scheme to manufacture a semiconductor device, comprising:

forming over a substrate a photo-definable layer that is convertible to an insulative material;

exposing selected portions of said photo-definable layer to electro-magnetic radiation in a ~~positive~~ negative pattern scheme to convert said selected portions to an insulative material;

removing non-exposed portions of said photo-definable layer with an etch process that is selective to exposed portions of said photo-definable layer;

using said ~~non-exposed~~ exposed portions of said photo-definable layer as a patterned mask for further processing steps, and

leaving said exposed portions of said photo-definable layer as an insulative layer within said semiconductor device.

56.(Previously Presented) The process of claim 55, wherein said photo-definable layer comprises an organosilicon resist.

57. (Previously Presented) The process of claim 56, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS) and said insulative material comprises photo-oxidized siloxane (PPMSO).

58. (Previously Presented) The process of claim 57, further comprising converting said PPMSO layer to oxide through exposure to an oxygen plasma.

59.(Amended) A semiconductor device formed using a photo-definable layer in a ~~positive~~ negative mask scheme, comprising:

a substrate;

at least one feature formed on said substrate by converting selected portions of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation in a negative mask scheme, by using exposed portions of said photo-definable layer as a mask to form said at least one feature, and by leaving said exposed portions of said photo-definable layer on said substrate as an insulative layer.

60. (Previously Presented) The semiconductor memory device of claim 59, wherein said photo-definable layer comprises an organosilicon resist.

61. (Previously Presented) The semiconductor memory device of claim 60, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS).

62.(Amended) A process for forming a self-aligned contact during the manufacture of a semiconductor device using a photo-definable layer in a ~~positive~~ negative mask scheme, comprising:

forming an insulative layer over a substrate having at least two spaced structures;

forming over said insulative layer a photo-definable layer that is convertible to an insulative material;

exposing selected portions of said photo-definable layer to electro-magnetic radiation in a ~~positive~~ negative pattern scheme to convert said selected portions to an insulative material;

removing non-exposed portions of said photo-definable layer with an etch process that is selective to exposed portions of said photo-definable layer to expose selected portions of said insulative layer between said spaced structures;

removing said selected portions of said insulative layer to expose underlying portions of said substrate; and

depositing conductive material to form a self-aligned contact between said spaced structures.

63. (Previously Presented) The process of claim 62, wherein said photo-definable layer comprises an organosilicon resist.

64. (Previously Presented) The process of claim 63, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS) and said insulative material comprises photo-oxidized siloxane (PPMSO).

65. (Previously Presented) The process of claim 64, further comprising converting said PPMSO to an oxide layer by exposure to oxygen plasma and consolidating said oxide layer with an anneal.

66. (Previously Presented) The process of claim 62, wherein said exposing step is performed by irradiating said selected portions of said photo-definable layer with ultraviolet light in the presence oxygen.

67. (Previously Presented) The process of claim 66, wherein said non-exposed portions of said photo-definable layer are removed using a chlorine-based or a bromine-based plasma etch.

68. (Previously Presented) The process of claim 66, wherein said insulative layer comprises an oxide layer and said insulative layer is removed using a short punch-through oxide etch.

69. (Previously Presented) The process of claim 62, wherein said spaced structures comprise transistor gate structures that are part of a memory cell array.

70. (Previously Presented) The process of claim 69, wherein said gate structure comprise a polysilicon layer and said insulative layer comprises an oxide layer.

71.(Amended) A self-aligned contact structure within a semiconductor device formed using a photo-definable layer in a ~~positive~~ negative mask scheme, comprising:

a substrate; and

at least one self-aligned contact formed on said substrate by converting selected portions of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation in a ~~positive~~ negative mask scheme and by using exposed portions of said photo-definable layer as a mask to form said at least one self-aligned contact.

72. (Previously Presented) The self-aligned contact structure of claim 71, further comprising an insulative layer formed by leaving said exposed portions of said photo-definable layer on said substrate.

73. (Previously Presented) The self-aligned contact structure of claim 72, wherein said photo-definable layer comprises an organosilicon resist.

74. (Previously Presented) The self-aligned contact structure of claim 73, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS).

75. (Previously Presented) The self-aligned contact structure of claim 71, where said at least one self-aligned contact lies between two transistor gate structures within a memory cell array.

76. (Previously Presented) A process of using a photo-definable layer in a Damascene process to create a patterned structure, comprising:

forming on a substrate a photo-definable layer that is convertible to an insulative material;

exposing selected portions of said photo-definable layer to electro-magnetic radiation to convert said selected portions to an insulative material;

removing non-exposed portions of said photo-definable layer with an etch process that is selective to exposed portions of said photo-definable layer to form a desired pattern within said exposed portions of said photo-definable layer; and

leaving said exposed portions of said photo-definable layer on said substrate as an insulative layer.

77. (Previously Presented) The process of claim 76, wherein said photo-definable layer comprises an organosilicon resist.

78. (Previously Presented) The process of claim 77, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS) and said insulative material comprises photo-oxidized siloxane (PPMSO).

79. (Previously Presented) The process of claim 78, further comprising converting said PPMSO to an oxide layer by exposure to oxygen plasma and consolidating said oxide layer with an anneal.

80. (Previously Presented) The process of claim 79, further comprising depositing a conductive material within said pattern.

81. (Previously Presented) The process of claim 80, wherein said conductive material forms an interconnect structure within a semiconductor memory device.

82. (Previously Presented) The process of claim 76, wherein said exposing step is performed by irradiating said selected portions of said photo-definable layer with ultraviolet light in the presence oxygen.

83. (Previously Presented) The process of claim 82, wherein said non-exposed portions of said photo-definable layer are removed using a chlorine-based or a bromine-based plasma etch.

84.(Amended) A conductive interconnect structure within a semiconductor device formed using a photo-definable layer, comprising:

a substrate;

a patterned insulative layer on said substrate formed by converting selected portions of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation in a ~~positive~~ negative mask scheme, by removing non-exposed portions of said photo-definable layer to form a pattern within said photo-definable layer, and by leaving said exposed portions of said photo-definable layer as said patterned insulative layer; and

a conductive layer inlaid within said patterned insulative layer.

85. (Previously Presented) The semiconductor structure of claim 84, wherein said photo-definable layer comprises an organosilicon resist.

86. (Previously Presented) The semiconductor structure of claim 85, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS).

87. (Previously Presented) The semiconductor structure of claim 83, wherein said conductive layer forms an interconnect structure within a semiconductor memory device.

88. (Previously Presented) A process of using a photo-definable layer in a dual Damascene process to create a patterned structure, comprising:

forming over a conductive layer a first photo-definable layer that is convertible to an insulative material;

exposing selected portions of said first photo-definable layer to electro-magnetic radiation to convert said selected portions to an insulative material to define desired contact areas;

forming over said first photo-definable layer a second photo-definable layer that is convertible to an insulative material;

exposing selected portions of said second photo-definable layer to electro-magnetic radiation to convert said selected portions to an insulative material to define a desired interconnect pattern; and

removing non-exposed portions of said first and second photo-definable layers to form voids exposing said desired contact areas and said desired interconnect pattern.

89. (Previously Presented) A process of claim 88, further comprising removing non-exposed portions of said first photo-definable layer to expose said desired contact areas before forming said second photo-definable layer.

90. (Previously Presented) The process of claim 88, wherein said photo-definable layer comprises an organosilicon resist.

91. (Previously Presented) The process of claim 90, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS) and said insulative material comprises photo-oxidized siloxane (PPMSO).

92. (Previously Presented) The process of claim 91, further comprising converting said PPMSO to an oxide layer by exposure to oxygen plasma and consolidating said oxide layer with an anneal.

93. (Previously Presented) The process of claim 92, further comprising depositing a conductive material within said voids.

94. (Previously Presented) The process of claim 93, wherein said conductive material forms digit-line connections for dynamic random access memory cells.

95. (Previously Presented) The process of claim 89, wherein said exposing steps are performed by irradiating said selected portions of said photo-definable layer with ultraviolet light in the presence oxygen.

96. (Previously Presented) The process of claim 95, wherein said non-exposed portions of said photo-definable layer are removed using a chlorine-based or a bromine-based plasma etch.

97.(Amended) A conductive interconnect structure within a semiconductor device, comprising:

a substrate;

a first conductive layer on said substrate;

a patterned insulative layer on said first conductive layer formed by converting selected portions of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation in a ~~positive~~ negative mask scheme, by removing non-exposed portions of said photo-definable layer to form a pattern within said photo-definable layer, and by leaving said exposed portions of said photo-definable layer as said patterned insulative layer; and

a second conductive layer inlaid within said insulative layer forming contacts with selected portions of said first conductive layer.

98. (Previously Presented) The semiconductor structure of claim 97, wherein said photo-definable layer comprises an organosilicon resist.